

Features of the MSP430 Bootstrap Loader

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MSP430

ABSTRACT

The MSP430 bootstrap loader (BSL) enables users to communicate with embedded memory in the MSP430 microcontroller during the prototyping phase, final production, and in service. Both the programmable memory (flash memory) and the data memory (RAM) can be modified as required.

The commonly used UART protocol with RS232 interfacing is supported, allowing flexible use of both hardware and software.

To use the bootstrap loader, a specific BSL entry sequence has to be applied to specific device pins. An added sequence of commands initiates the desired function. A boot loading session can be exited by continuing operation at a defined user program address, or by the reset condition.

Access to the MSP430 memory via the bootstrap loader is protected against misuse by a user-defined password.

Contents

1	Introduction.....	2
2	Standard RESET and BSL Entry Sequence	3
	2.1 MSP430 20- and 28-Pin Flash Devices With Shared JTAG Pins	3
	2.2 MSP430 Flash Devices With Dedicated JTAG Pins	4
3	UART Protocol	4
4	Synchronization Sequence	4
5	Commands	5
	5.1 Unprotected Commands	5
	5.2 Password Protected Commands	5
6	Programming Flow	5
7	Data Frame	5
	7.1 Data Stream Structure	6
	7.2 Checksum	6
	7.3 Commands - Detailed Description.....	7
	7.3.1 General	7
	7.3.2 RX Data Block.....	7
	7.3.3 RX Password.....	8
	7.3.4 Mass Erase	8
	7.3.5 Erase Segment.....	8
	7.3.6 Erase Check.....	9
	7.3.7 Change Baud Rate.....	9
	7.3.8 Load PC	10
	7.3.9 TX Data Block	10
	7.3.10 TX BSL Version.....	11

8	Loadable BSL	11
9	Exiting the BSL	12
10	Password Protection	12
11	Code Protection Fuse	12
12	BSL Internal Settings and Resources	12
	12.1 Chip Identification and BSL Version.....	13
	12.2 Vectors.....	13
	12.3 Initialization Status.....	13
	12.4 Memory Allocation and Resources.....	14
13	Special Consideration for BSL Version 1.10	15
14	References	15
	Appendix A. Differences Between Devices and BSL Versions	16

Figures

Figure 1.	Standard RESET Sequence	3
Figure 2.	BSL Entry Sequence	3
Figure 3.	BSL Entry Sequence at Dedicated JTAG Pins	4

Tables

Table 1.	Data Frame of BSL Commands	6
Table 2.	Recommendations for MSP430F149 [F449] ($T_A = 25^\circ\text{C}$, $V_{CC} = 3.0\text{ V}$, $f_{max} = 6.7\text{ MHz}$)	10
Table 3.	BSL Version 1.10 on F13x, F14x, F11x, and F11x1	16
Table 4.	BSL Version 1.30 on F41x, F11x, and F11x1	17
Table 5.	BSL Version 1.40 on F12x	18
Table 6.	BSL Version 1.50 on F43x and F44x	19
Table 7.	BSL Version 1.60 on F12x2, F43x, and F44x	20

1 Introduction

This bootstrap loader (BSL) provides a method to program the flash memory during MSP430 project development and updates. It can be activated by a utility that sends commands via the familiar UART protocol. The BSL enables the user to control the activity of the MSP430 and to exchange data using a personal computer or other device that supports a UART protocol.

To avoid accidental overwriting of the BSL code, this code is stored in a special factory-masked boot ROM. The BSL cannot ever be erased. The BSL code is highly optimized for the BSL function and is accessed using commands described later in this document. For security purposes and to prevent unwanted source readout, user code protection is very important. Any BSL command that directly or indirectly allows data reading is password protected.

To invoke the bootstrap loader, a BSL entry sequence has to be applied to dedicated pins. After that, a synchronization character, followed by the data frame of a specific command, initiates the desired function.

2 Standard RESET and BSL Entry Sequence

2.1 MSP430 20- and 28-Pin Flash Devices With Shared JTAG Pins

Applying an appropriate entry sequence on the -RST/NMI and TEST pins forces the MSP430 to start program execution at the BSL RESET vector instead of at the RESET vector located at address FFFEH.

If the application interfaces with a computer UART, these two pins may be driven by the -DTR and -RTS signals of the serial communication port (RS232) after passing level shifters. Detailed descriptions of the hardware and related considerations are given in a separate document (see *References*, Section 14). The normal user reset vector at FFFEH is used, if TEST is kept low while RST/NMI rises from low to high (standard method, see Figure 1).

The BSL program execution starts whenever the TEST pin has received a minimum of two positive transitions and if TEST is high while -RST/NMI rises from low to high (BSL entry method, see Figure 2). This level/transition triggering improves BSL startup reliability.

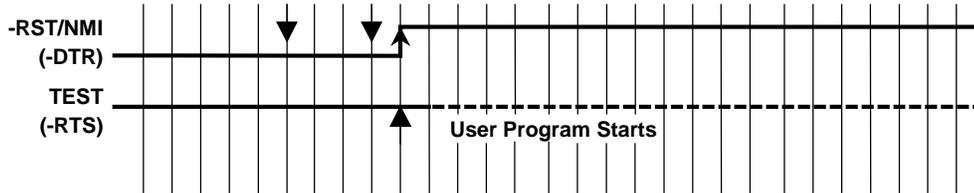


Figure 1. Standard RESET Sequence

The TEST signal is normally used simply to switch the port pins P1.7 – P1.4 between their application function and the JTAG function. If the second rising edge at the TEST pin is applied while -RST/NMI is still low, the TEST signal is kept low internally (application mode).

The BSL will not be started (via the BSL RESET vector), if:

- There are less than two positive edges at the TEST pin while -RST/NMI is low
- TEST is low when -RST/NMI rises from low to high
- JTAG has control over the MSP430 resources
- Supply voltage V_{CC} drops down and a power-on reset (POR) is executed

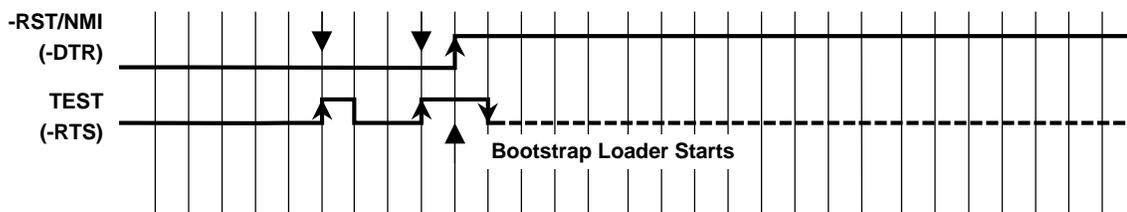


Figure 2. BSL Entry Sequence

2.2 MSP430 Flash Devices With Dedicated JTAG Pins

Devices with dedicated JTAG pins use the TCK pin instead of the TEST pin.

The BSL program execution starts whenever the TCK pin has received a minimum of two negative transitions and TCK is low while -RST/NMI rises from low to high (BSL entry method, see Figure 3). This level/transition triggering improves BSL start-up reliability.

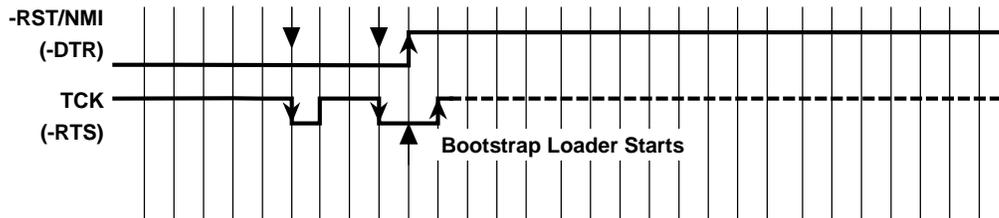


Figure 3. BSL Entry Sequence at Dedicated JTAG Pins

The BSL will not be started (via the BSL RESET vector), if:

- There are less than two negative edges at TCK pin while -RST/NMI is low
- TCK is high if -RST/NMI rises from low to high
- JTAG has control over the MSP430 resources
- Supply voltage VCC drops down and a power on reset (POR) is executed

3 UART Protocol

The UART protocol applied here is defined as:

- Baud rate is fixed to 9600 baud in half duplex mode (one sender at a time).
- Start bit, 8 data bits, an even parity bit, 1 stop bit.
- Handshake is performed by an acknowledge character.

NOTE: Applying baud rates other than 9600 baud results in communication problems or violates the flash memory write timing specification. The flash memory may be extensively stressed or may react with unreliable program/erase operations.

4 Synchronization Sequence

Before receiving any command, a synchronization character (SYNC) with its value of 80h has to be received by the BSL. This character is necessary to calculate all the essential internal parameters, which maintain UART and flash memory programming/erasing timings. It provides the BSL system time reference.

Next, an acknowledge DATA_ACK = 90h is sent back by the BSL to confirm successful reception.

5 Commands

Two categories of commands are available: commands needing a password and commands that do not require a password. The password protection safeguards every command that *potentially allows direct or indirect data access*.

5.1 Unprotected Commands

- Receive password
- Mass erase
- Transmit BSL version (V1.50 or higher or in loadables BL_150S_14x.txt, BL_150S_44x.txt)
- Change baud rate (V1.60 or higher or in loadables BL_150S_14x.txt, BL_150S_44x.txt)

5.2 Password Protected Commands

- Receive data block to program flash memory, RAM, or peripherals
- Transmit data block
- Erase segment
- Erase check (V1.50 or higher or in loadables BL_150S_14x.txt, BL_150S_44x.txt)
- Load program counter and start user program

6 Programming Flow

The write access (RX data block command) to the flash memory/RAM or peripheral modules area is executed *online*. That means a data byte/word is processed immediately after receipt and the write cycle is finished before a following byte/word has completely arrived. Therefore, the entire write time is determined by the baud rate and no buffering mechanism is necessary.

Data sections located below the flash memory area address are assumed to be loaded into the RAM or peripheral module area, and thus no specific flash control bits are affected.

NOTE: When losing control over the UART protocol either by line faults or by violating the data frame conventions, the only way to recover is to rerun the BSL entry sequence to initiate another BSL session.

7 Data Frame

The data frame used follows the TI MSP430 serial standard protocol (SSP) rules extended with a preceding synchronization sequence (SS) as previously described. The BSL is considered as a receiver in Table 1.

The obvious redundancy of some parameters results from the adaptation to the SSP or to save boot ROM space.

7.1 Data Stream Structure

- The first 8 bytes (HDR through LH) are mandatory (xx represents dummy data).
- Data bytes D1 to Dn are optional.
- Two bytes (CKL and CKH) for checksum are mandatory.
- Acknowledge done by the BSL is mandatory except with the TX data block command.

7.2 Checksum

The 16-bit (2 bytes) checksum is calculated over all received/transmitted bytes B1 ... Bn in the data frame except the checksum bytes themselves by XORing words (2 successive bytes) and inverting the result.

Formula:

$$\text{CHECKSUM} = \text{INV} [(B1 + 256*B2) \text{ XOR } (B3 + 256*B4) \text{ XOR } \dots \text{ XOR } (B_{n-1} + 256*B_n)]$$

or

$$\text{CKL} = \text{INV} [B1 \text{ XOR } B3 \text{ XOR } \dots \text{ XOR } B_{n-1}] ; \quad \text{CKH} = \text{INV} [B2 \text{ XOR } B4 \text{ XOR } \dots \text{ XOR } B_n]$$

Table 1. Data Frame of BSL Commands

Received BSL Command	HDR	CMD	L1	L2	AL	AH	LL	LH	D1	D2 ... Dn	CKL	CKH	ACK
RX data block	80	12	n	n	AL	AH	n-4	0	D1	D2 ... Dn-4	CKL	CKH	ACK
RX password	80	10	24	24	xx	xx	xx	xx	D1	D2 ... D20	CKL	CKH	ACK
Erase segment	80	16	04	04	AL	AH	02	A5	—	— — —	CKL	CKH	ACK
Mass erase	80	18	04	04	xx	xx	xx	xx	—	— — —	CKL	CKH	ACK
Erase check	80	1C	04	04	AL	AH	LL	LH	—	— — —	CKL	CKH	ACK
Change baud rate	80	20	04	04	D1	D2	D3	xx	—	— — —	CKL	CKH	ACK
Load PC	80	1A	04	04	AL	AH	xx	xx	—	— — —	CKL	CKH	ACK
TX data block	80	14	04	04	AL	AH	n	0	—	— — —	CKL	CKH	—
BSL responds	80	xx	n	n	D1	D2... Dn	CKL	CKH	—
TX BSL version	80	1E	04	04	xx	xx	xx	xx	—	— — —	CKL	CKH	—
BSL responds	80	xx	10	10	D1	D2... D10	CKL	CKH	—

Notes: All numbers are bytes in hexadecimal notation.

ACK is sent back by the BSL.

The synchronization sequence is not part of the data frame.

The erase check and TX BSL version commands are not members of the standard command set (V1.50 or higher).

The change baud rate command is not a member of the standard command set (V1.60 or higher or in loadables BL_150S_14x.txt, BL_150S_44x.txt).

Abbreviations:

HDR DATA_FRAME = 80h means *data frame expected* in accordance with TI MSP430 serial standard protocol (SSP).

CMD Command identification

L1, L2 Number of bytes consisting of AL through Dn
Restrictions: L1 = L2, L1 < 255, L1 even.

AL, AH Block start address or erase (check) address or jump address LO/Hi byte

LL, LH Number of pure data bytes (max. 250) or erase information LO/Hi byte or block length of erase check (max. FFFFh)

D1 ... Dn Data bytes

CKL, CKH 16-bit checksum LO/Hi byte

xx Can be any data

-- No character (data byte) received/transmitted

ACK The acknowledge character returned by the BSL, can be either
 DATA_ACK = 90h: Frame was received correctly, command was executed successfully, or
 DATA_NAK = A0h: Frame not valid (e.g., wrong checksum, L1 ≠ L2),
 command is not defined, is not allowed, or was executed unsuccessfully.

n Number of bytes consisting of AL through Dn

7.3 Commands - Detailed Description

See Table 1.

7.3.1 General

Besides the header byte HDR (80h) and the command identification CMD, the frame length bytes L1 and L2 (which must be equal) hold the number of bytes following L2, excluding the checksum bytes CKL and CKH.

Bytes AL, AH, LL, LH, D1...Dn are command-specific. However, the checksum bytes CKL (low byte) and CKH (high byte) are mandatory.

If the data frame has been received correctly and the command execution was successful, an acknowledge character DATA_ACK = 90h is sent back by the BSL. Incorrectly received data frames, unsuccessful operations, commands which are locked or not defined are confirmed with a DATA_NAK = A0h.

NOTE: BSL versions lower than V1.30 support only byte access operations. The peripheral module addresses at 0100h–01FFh thus cannot be accessed correctly because they are word-oriented. From version V1.30 on addresses 0000h–00FFh are accessed in byte mode; all others are accessed in word mode.

7.3.2 RX Data Block

The receive data block command is used for any write access to the flash memory/RAM or peripheral module control registers at 0000h–01FFh. It is password protected.

The 16-bit even-numbered block start address is defined in AL (low byte) and AH (high byte). The 16-bit even-numbered block length is defined in LL (low byte) and LH (high byte). Because pure data bytes are limited to a maximum of 250, LH is always 0.

The following data bytes are succeeded by the checksum bytes CKL (low byte) and CKH (high byte). If the receipt and programming of the appropriate data block was successful, an acknowledge character DATA_ACK is sent back by the BSL. Otherwise, the BSL confirms with a DATA_NAK.

NOTE: BSL versions V1.40 and higher support online verification inside the MSP430 for addresses 0200h–FFFFh which reduces programming/verification time to 50 percent. In case of an error the loadable bootstrap loaders BL_150S_14x.txt and BL_150S_44x.txt additionally store the first incorrectly written location address+3 into the error address buffer in the RAM at address 0200h (021Eh for F14x devices).

7.3.3 RX Password

The receive password command is used to unlock the password-protected commands, which perform reading, writing, or segment-erasing memory access. It is not password protected.

Neither start address nor block length information is necessary because the 32-byte password is always located at addresses FFE0h–FFFFh. Data bytes D1 to D20h hold the password information starting with D1 at address FFE0h.

If the receipt and verification of the password is correct a positive acknowledge DATA_ACK is sent back by the BSL and the password-protected commands become unlocked. Otherwise the BSL confirms with a DATA_NAK.

Once the protected commands become unlocked they remain unlocked until another BSL entry is initiated.

7.3.4 Mass Erase

The mass erase command erases the entire flash memory area (main memory plus information memory, see corresponding data sheet). It is not password protected.

All parameters shown in Table 1 are mandatory. After erasing, an acknowledge character DATA_ACK is sent back by the BSL.

Mass erase initializes the password area to 32 times 0FFh.

7.3.5 Erase Segment

The erase segment command erases specific flash memory segments. It is password protected.

The address bytes AL (low byte) and AH (high byte) select the appropriate segment. Any even-numbered address within the segment to be erased is valid. After segment erasing, an acknowledge character DATA_ACK is sent back by the BSL (V1.40 or lower).

BSL versions V1.50 or higher perform a subsequent erase check of the corresponding segment and respond with a DATA_NAK if the erasure was not successful. In this case the first not erased location address+1 is stored in the error address buffer in the RAM at address 0200h (021Eh for F14x devices).

Erase segment 0 clears the password area, and therefore the remaining password is 32 times 0FFh.

The MSP430Fxxxx device segmentation is configured as follows:

0FE00h–0FFFFh :	Segment 0	Main memory
0FC00h–0FDFFh :	Segment 1	
0FA00h–0FBFFh :	Segment 2	
0F800h–0F9FFh :	Segment 3	
		...
		...
01200h–013FFh :	Segment n-1	
01100h–011FFh :	Segment n	
01080h–010FFh :	Segment A	Information memory
01000h–0107Fh :	Segment B	

7.3.6 Erase Check

The erase check command verifies the erasure of flash memory within a certain address range. It is password protected.

The 16-bit block start address is defined in AL (low byte) and AH (high byte). The 16-bit block length is defined in LL (low byte) and LH (high byte). Both can be either even or odd numbered to allow odd boundary checking.

If the erase check of the appropriate data block was successful (all bytes contain 0FFh), an acknowledge character DATA_ACK is sent back by the BSL. Otherwise the BSL confirms with a DATA_NAK and the first not erased location address+1 is stored in the error address buffer at address 0200h (021Eh for F14x devices).

NOTE: This command is not a member of the standard command set. It is implemented from BSL version V1.50 on or in the loadable bootstrap loaders BL_150S_14x.txt and BL_150S_44x.txt.

7.3.7 Change Baud Rate

The change baud rate command offers the capability of transmissions at higher baud rates than the default 9600 baud. With faster data transition shorter programming cycles can be achieved which is especially important with large flash memory devices. This command is not password protected.

Three control bytes D1 to D3 determine the selected baud rate. D1 and D2 set the processor frequency ($f \geq f_{min}$), D3 indirectly sets the flash timing generator frequency ($f_{TGmin} \leq f_{TG} \leq f_{TGmax}$). In detail:

- D1: F1xx: Basic clock module control register DCOCTL (DCO.2 ... DCO.0)
F4xx: FLL+ system clock control register SCFI0 (D, FN_8 ... FN_2)
- D2: F1xx: basic clock module control register BCSCCTL1 (XT2Off, Rsel.2 ... Rsel.0)
F4xx: FLL+ system clock control register SCFI1 (N_{DCO})
- D3: 0: 9600 Baud
1: 19200 Baud
2: 38400 Baud

After receiving the data frame an acknowledge character DATA_ACK is sent back and the BSL becomes prepared for the selected baud rate. It is recommended for the BSL communication program to wait a little while (approximately 10 ms) between baud rate alternation and succeeding data transmission to give the BSL clock system time for stabilization.

NOTE: The highest achievable baud rate depends on various system and environment parameters like supply voltage, temperature range, and minimum/maximum processor frequency. See the corresponding device specification / data sheet.

NOTE: This command is implemented on BSL versions V1.60 or higher or available in the loadable bootstrap loaders BL_150S_14x.txt and BL_150S_44x.txt.

**Table 2. Recommendations for MSP430F149 [F449] (T_A = 25°C, V_{CC} = 3.0 V, f_{max} = 6.7 MHz)
(see Note 2)**

Baud Rate (Baud)	Proc. Freq. f _{min} (MHz) (see Note 4)	D1 DCOCTL [SCFI0] (see Note 1)	D2 BCSCCTL1 [SCFI1] (see Note 1)	D3 (see Note 1)	Progr. / Verify 60 Kbytes (sec) (see Note 3)
9600 (init)	1.05	80 [00]	85 [98]	00 [00]	78 + 3.7 [0.0]
19200	2.1	E0 [00]	86 [B0]	01 [01]	39 + 3.7 [2.4]
38400	4.2	E0 [00]	87 [C8]	02 [02]	20 + 3.7 [2.4]

- Notes:
1. D1 to D3 are bytes in hexadecimal notation.
 2. Values in brackets [] are related to MSP430F449.
 3. Additional 3.7 [2.4] seconds result from loading, verifying, and launching the loadable BSL.
 4. The minimum processor frequency is lower than in the standard ROM BSL (see *Initialization Status*, Section 12.3).

7.3.8 Load PC

The load program counter command directs the program counter (register R0) to any location within the entire address range. It is password protected.

After receiving the data frame an acknowledge character DATA_ACK is sent back by the BSL. Then the selected address is moved into the program counter. The program flow continues operation there, and the BSL session is terminated.

Be aware that the password protection is not active at this time.

7.3.9 TX Data Block

The transmit data block command is used for any read access to the flash memory/RAM or peripheral module control registers at 0000h–01FFh. It is password protected.

The 16-bit block start address is defined in AL (low byte) and AH (high byte). The 16-bit block length is defined in LL (low byte) and LH (high byte). Because pure data bytes are limited to a maximum of 250, LH is always 0. The checksum bytes CKL (low byte) and CKH (high byte) immediately follow this information.

Now the BSL responds with the requested data block. After transmitting HDR, dummy CMD, L1 and L2, The BSL sends data bytes D1 through Dn, followed by the checksum bytes CKL (low byte) and CKH (high byte). No acknowledge character is necessary.

7.3.10 TX BSL Version

The transmit BSL version command gives the user information about chip identification and bootstrap loader software version. It is not password protected.

The values for AL, AH, LL, and LH can be any data, but must be transmitted to meet the protocol requirements. The checksum bytes CKL (low byte) and CKH (high byte) immediately follow this information.

After that, the BSL responds with a 16-byte data block. After transmitting HDR, dummy CMD, L1 and L2, the BSL sends data bytes D1 through D16 (decimal), followed by the checksum bytes CKL (low byte) and CKH (high byte). No acknowledge character is necessary.

D1, D2 and D11, D12 (decimal) hold the specific information:

- D1: Device family type (high byte)
- D2: Device family type (low byte)
- D11: BSL version (high byte)
- D12: BSL version (low byte)

The remaining 12 bytes are for internal use only.

8 Loadable BSL

For upgrading the BSL functionality, sometimes it is suitable to load a higher version of BSL into the RAM of a device and apply the latest innovations. To do so, use the following BSL commands:

- RX password (unlock password protection for following commands)
- RX data block (code of loadable BSL, code section address \geq 220h)
- TX data block (for verification)
- RX data block (get start address from first code section address)
- Load program counter PC (with start address of loadable BSL)
- RX password (unlock password protection for loaded BSL)
- Perform any command (with loaded BSL)

For more information on downloading a different bootstrap loader, see *Application of Bootstrap Loader in MSP430 With Flash Hardware and Software Proposal* (SLAA096B).

Third party software normally uses loadable BSLs to perform most functions, like online verification, and to improve speed for appropriate devices.

9 Exiting the BSL

To exit the BSL mode two possibilities are provided:

- The microcontroller continues operation at a defined program address invoked by the load program counter command. Be aware of that the password protection is not active at this time.
- Applying the standard RESET sequence (see Figure 1) forces the MSP430 to start with the user reset vector at address 0FFFEh.

10 Password Protection

The password protection prohibits every command that potentially allows direct or indirect data access. Only the unprotected commands like mass erase and RX password (optionally TX BSL version, change baud rate) can be performed without prior receipt of the correct password after BSL entry.

Applying the RX password command for receiving the correct password unlocks the remaining commands.

Once it is unlocked it remains unlocked until initiating another BSL entry. A reset condition ($-RST/NMI = 0 \rightarrow 1$, $V_{CC} = 0 \rightarrow 1$) has no influence on the protection behavior.

The password itself consists of the 16 interrupt vectors located at addresses FFE0h to FFFFh (256 bits) starting with the first byte at address FFE0h. After mass erase and with unprogrammed devices, all password bits are logical high (1).

NOTE: The user has to take care of password update after modifying the interrupt vectors and initiating another BSL session. It is also strongly recommended to initialize unused interrupt vectors to increase data safety.

11 Code Protection Fuse

Once the JTAG fuse (code protection fuse) is blown, no further access to the JTAG/test feature is possible. The only way to get any memory read/write access is via the bootstrap loader by applying the correct password.

However, it is not possible for the BSL to blow the JTAG fuse. If fuse blowing is needed, use JTAG programming techniques.

12 BSL Internal Settings and Resources

The following paragraphs describe BSL internal settings and resources. Because the same device may have implemented different BSL versions, it is very important for the BSL communication program to know the settings and resources. Resources could be either device dependent (e.g., RX/TX pins) or BSL-version dependent (e.g., byte/word access). The following paragraphs, therefore, distinguish among the possible variations.

12.1 Chip Identification and BSL Version

The upper 16 bytes of the boot-ROM (0FF0h–0FFFh) hold information about the device and BSL version number in BCD representation. This is common for all devices and BSL versions:

- 0FF0h–0FF1h: Chip identification (e.g., F413h for an F41x device).
- 0FFAh–0FFBh: BSL version number (e.g. 0130h for BSL version V1.30).

Please see the MSP430 device / BSL version assignment in Appendix A.

12.2 Vectors

The entry part of the boot ROM holds the calling vectors for BSL access by program:

- 0C00h: Vector for cold-start (mnemonic: *BR &0C00h*)
- 0C02h: Vector for warm-start (mnemonic: *BR &0C02h*). *V1.30 or higher.*
- 0C04h: Vector(s) for future use. This table is expandable.

12.3 Initialization Status

When activating the BSL, the following settings come into effect:

- Stop Watchdog Timer
- Disable all interrupts (GIE=0)
- V1.10:
The stack pointer is not modified except when it points to an excluded memory area. If so, it is initialized to 021Ah.
V1.30 or higher:
The stack pointer is not modified if the BSL is called by program via the warm-start vector. It is initialized to 0220h if the BSL starts via the BSL RESET sequence or is called by program via the cold-start vector.
- F1xx:
Determine basic clock module so that minimum frequency is 1.5 MHz:
BCSCTL1 = 85h (RSEL = 5, XT2Off = 1)
DCOCTL = 80h (DCO = 4, MOD = 0)

F4xx:
Determine FLL oscillator/system clock so that minimum frequency is 1.5 MHz:
SCFI0 = 00h (D = 0, FN_x = 0)
SCFI1 = 98h (N_DCO)
SCFQCTL: (M = 0)
SR: SCG0 = 1 (FLL loop control off)
- SW-UART: Timer_A operates in continuous mode with MCLK source (Div = 1)
CCR0 used for compare
CCTL0 used for polling of CCIFG0

- TX pin is set to output HI for RS232 idle state
- RX pin is set to input
- Password protected commands are locked (only at cold-start)

After system initialization, the BSL is ready for operation and waits for the first synchronization sequence (SS) followed by a data frame containing the first BSL command.

12.4 Memory Allocation and Resources

- The BSL program code is located in the boot-ROM area 0C00h–0FEFh.
- Addresses 0FF0h–0FFFh hold the device identification
- The BSL variables occupy the RAM area
0200h–0213h (V1.10)
0200h–0219h (V1.30 or higher).
- The BSL stack occupies the RAM area
0214h–0219h (V1.10)
021Ah–021Fh (V1.30 or higher, only at cold-start).
- The working registers used are
R5–R9 (V1.30 or lower) or
R5–R10 (V1.40) or
R5–R11 (V1.50).
Their contents are not buffered.
- F1xx:
The basic clock module registers used are:
DCOCTL at address 056h
BCSCTL1 at address 057h

F4xx:
The FLL oscillator/system clock registers used are:
SCFI0 at address 050h
SCFI1 at address 051h
SCFQCTL at address 052h

The Timer_A control registers used are:
TACTL at address 0160h
CCTL0 at address 0162h
TAR at address 0170h
CCR0 at address 0172h
- No interrupt service is affected.

13 Special Consideration for BSL Version 1.10

The first official version V1.10 of the BSL requires a small loadable patch sequence, PATCH.TXT, to execute the RX block command reliably. For that, after the BSL has been started, proceed in the following manner:

- RX password (unlock password protection for the following command)
- Load program counter (PC) with 0C22h (initialize stack pointer to a safe address)
- RX password again (unlock password protection for subsequent commands)
- RX data block (code of loadable patch, code section address is 0220h)
- TX data block (code of loadable patch for verification)

From now on, the RX block and TX block commands can be used with one restriction: Prior to their invocation the program counter must be set to the start address of the patch.

- Load program counter (PC) with start address 0220h of loadable patch
- RX data block (code to be programmed at any location) -or-
- TX data block (from any location)

For more information on downloading a patch or different bootstrap loader, see *Application of Bootstrap Loader in MSP430 With Flash Hardware and Software Proposal* (SLAA096).

14 References

1. *MSP430x1xx Family User's Guide* (SLAU049)
2. *MSP430x4xx Family User's Guide* (SLAU056)
3. *MSP430 Family Software User's Guide* (SLAUE11)
4. *Application of Bootstrap Loader in MSP430 With Flash Hardware and Software Proposal* (SLAA096)

For a list of third parties that offer BSL hardware and software solutions, please see the MSP430 web site at <http://www.ti.com/sc/msp430>.

Appendix A. Differences Between Devices and BSL Versions

As a summary the tables in this chapter show the key information of MSP430 device/BSL version assignment related to their hard/software resources.

Table 3. BSL Version 1.10 on F13x, F14x, F11x, and F11x1

Device		F13x F14x	F11x F11x1
BSL Version		1.10	
BSL vector address	Cold start	0C00h	
	Warm start	—	
Chip ID address		0FF0h	
Chip ID data		F149h	F112h
BSL version address		0FFAh	
BSL version data		0110h	
Mass erase time, nominal (ms)		17.2	
Read/write access at 0000h–FFFFh		Byte	
Verification during write (online)		No	
Stack pointer initialization	SP critical	021Ah	
	SP not critical	Unchanged	
Resources used by BSL			
Transmit pin (TX) / Receive pin (RX)		P 1.1 / P2.2	
RAM/stack used		0200h–0219h	
Working registers		R5–R9	
System clock, affected controls		BCSCTL1, DCOCTL	
Timer_A, affected controls		TACTL, TAR, CCTL0, CCR0	
Preparation for SW call		<pre> mov #00h, &CCTL0 bic.b #02h, &P1SEL bic.b #04h, &P2SEL bic.b #32h, &IE1 br &0C00h </pre>	
Comment 1	Workaround mandatory:	Load PATCH.TXT to eliminate ROM bug.	
Comment 2	Optional for F148, F149 only: Use loadable BSL (>1KB RAM required)	Load BL_150S_14x.txt to get all features of V1.50 plus change baud rate command.	

Table 4. BSL Version 1.30 on F41x, F11x, and F11x1

Device		F41x	F11x F11x1
BSL Version		1.30	
BSL vector address	Cold start	0C00h	
	Warm start	0C02h	
Chip ID address		0FF0h	
Chip ID data		F413h	F112h
BSL version address		0FFAh	
BSL version data		0130h	
Mass erase time, nominal (ms)		206.4	
Read/write access at	0000h–00FFh	Byte	
	0100h–FFFEh	Word	
Verification during write (online)		No	
Stack pointer initialization	Cold start	0220h	
	Warm start	Unchanged	
Resources used by BSL			
Transmit pin (TX)		P 1.0	P 1.1
Receive pin (RX)		P 1.1	P 2.2
RAM/stack used		0200h–021Fh	
Working registers		R5–R9	
System clock, affected controls		SCF10, SCF11, SCFQCTL	BCSCTL1, DCOCTL
Timer_A, affected controls		TACTL, TAR, CCTLO, CCR0	
Preparation for SW call		mov #00h, &CCTL0 br &0C00h	

Table 5. BSL Version 1.40 on F12x

Device		F12x
BSL Version		1.40
BSL vector address	Cold start	0C00h
	Warm start	0C02h
Chip ID address		0FF0h
Chip ID data		F123h
BSL version address		0FFAh
BSL version data		0140h
Mass erase time, nominal (ms)		206.4
Read/Write access at	0000h–00FFh	Byte
	0100h–FFFEh	Word
Verification during Write (online)		For addresses 0200h–FFFEh
Stack pointer initialization	Cold start	0220h
	Warm start	Unchanged
Resources used by BSL		
Transmit pin (TX)		P 1.1
Receive pin (RX)		P 2.2
RAM/stack used		0200h–021Fh
Working registers		R5–R10
System clock, affected controls		BCSCTL1, DCOCTL
Timer_A, affected controls		TACTL, TAR, CCTLO, CCR0
Preparation for SW call		br &0C00h

Table 6. BSL Version 1.50 on F43x and F44x

Device		F43x, F44x
BSL Version		1.50
BSL Vector Address	Cold start	0C00h
	Warm start	0C02h
Chip ID address		0FF0h
Chip ID data		F449h
BSL version address		0FFAh
BSL version data		0150h
Mass erase time, nominal (ms)		206.4
Read/write access at	0000h–00FFh	Byte
	0100h–FFFEh	Word
Verification during write (online)		For addresses 0200h–FFFEh
Erase Check command		Yes (error addr 0200h)
Erase Segment command		With erasure verification (error addr 0200h)
TX identification command		Yes
Change baud rate command		No
Stack pointer initialization	Cold start	0220h
	Warm start	unchanged
Resources used by BSL		
Transmit pin (TX)		P 1.0
Receive pin (RX)		P 1.1
RAM/stack used		0200h–021Fh
Working registers		R5–R11
System clock, affected controls		SCFI0, SCFI1, SCFQCTL
Timer_A, affected controls		TACTL, TAR, CCTL0, CCR0
Preparation for SW call		br &0C00h
Comment 1	Erase segment command	Addresses 1000h to 11FFh are verified coherently (3 segments). Also use erase check command.
Comment 2	Optional for F448, F449 only: Use loadable BSL (>1KB RAM required)	Load BL_150S_44x.txt to get change baud rate command and fix of comment 1.

Table 7. BSL Version 1.60 on F12x2, F43x, and F44x

Device		Preliminary F12x2	Preliminary F43x, F44x
BSL Version		1.60	
BSL vector address	Cold start	0C00h	
	Warm start	0C02h	
Chip ID address		0FF0h	
Chip ID data		1232h	F449h
BSL version address		0FFAh	
BSL version data		0160h	
Mass erase time nom. (ms)		206.4	
Read/write access at	0000h–00FFh	Byte	
	0100h–FFFEh	Word	
Verification during Write (online)		For addresses 0200h–FFFEh	
Erase check command		Yes (error addr 0200h)	
Erase segment command		With erasure verification (error addr 0200h)	
TX identification command		Yes	
Change baud rate command		Yes	
Stack pointer initialization	Cold start	0220h	
	Warm start	Unchanged	
Resources used by BSL			
Transmit pin (TX)		P 1.1	P1.0
Receive pin (RX)		P 2.2	P1.1
RAM/stack used		0200h–021Fh	
Working registers		R5–R12	
System clock, affected controls		BCSCTL1, DCOCTL	SCFI0, SCFI1, SCFQCTL
Timer_A, affected controls		TACTL, TAR, CCTL0, CCR0	
Preparation for SW call		br &0C00h	
Comment	Erase segment command	Addresses 1000h to 11FFh are verified coherently (3 segments). Also use erase check command.	

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